SPECIFICATIONS

PXIe-5763

16-Bit, 500 MS/s, 4-Channel PXI FlexRIO Digitizer

This document lists the specifications for the PXIe-5763. Specifications are subject to change without notice. For the most recent device specifications, refer to *ni.com/support*.

Contents

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

NATIONAL INSTRUMENTS

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ± 5 °C
- Installed in chassis with slot cooling capacity ≥58 W

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <3..0>[1]	Xilinx UltraScale GTH	Output
MGT Rx± <3..0>[1]	Xilinx UltraScale GTH	Input
DIO <7..0>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal

[1] Multi-gigabit transceiver (MGT) signals are available on devices with KU040 and KU060 FPGAs only.

Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[2]

Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA

Digital I/O High-Speed Serial MGT[3]

Note MGTs are available on devices with KU040 and KU060 FPGAs only.

Data rate	500 Mbps to 16.375 Gbps, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O AC coupling capacitor	100 nF

MGT TX± Channels

Minimum differential output voltage[4]	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled with 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
> 6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal

[2] Voltage levels are guaranteed by design through the digital buffer specifications.
[3] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.
[4] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor ⚠

Reconfigurable FPGA

PXIe-5763 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PXIe-5763 FPGA options.

Table 3. Reconfigurable FPGA Options

	KU035	KU040	KU060
LUTs	203,128	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,700	1,920	2,760
Embedded Block RAM	19.0 Mb	21.1 Mb	38.0 Mb
Default timebase	80 MHz		
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)		
Data transfers	DMA, interrupts, programmed I/O	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA channels	60		

Note The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Note For FPGA designs using the majority of KU040 or KU060 FPGA resources while running at clock rates over 150 MHz, the module may require more power than is available. If the module attempts to draw more than allowed per its specification, the module protects itself and reverts to a default FPGA personality. Refer to the getting started guide for your module or contact NI support for more information.

Onboard DRAM

Note DRAM is available on devices with KU040 and KU060 FPGAs only.

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Analog Input

Notice The maximum input signal levels are valid only when the module is powered on. To avoid permanent damage to the PXIe-5763, do not apply a signal to the device when the module is powered down.

General Characteristics

Number of channels	4, single-ended, simultaneously sampled
Connector type	SMA
Input impedance	50 Ω
Input coupling	AC or DC[5]
Sample Rate	
Internal Sample Clock	500 MHz
External Sample Clock	500 MHz[6]
Analog-to-digital converter (ADC)	ADS54J69, 16-bit resolution

Typical Specifications

Full-scale input range (normal operating conditions)	
AC-coupled	2.03 V_{pp} (10.15 dBm) at 10 MHz
DC-coupled	1.97 V_{pp} (9.87 dBm)

[5] Only one analog input path type is populated.
[6] You must provide a 1 GHz clock at the CLK/REF IN front panel connector to enable this rate.

Gain accuracy	
AC-coupled	±0.1 dB at 10 MHz
DC-coupled	±1% at DC
DC Offset	
AC-coupled	±41 µV
DC-coupled	±225 µV
Bandwidth (-3 dB)[7]	
AC-coupled	0.07 MHz to 225 MHz
DC-coupled	DC to 225 MHz[9]

Table 4. Single-Tone Spectral Performance

	AC-Coupled		DC-Coupled	
	Input Frequency		Input Frequency	
	10.1 MHz	123.1 MHz	10.1 MHz	123.1 MHz
SNR[9] (dBFS)	73.7	71.8	71.7	70.6
SINAD[9] (dBFS)	73.5	71.7	70.7	70.5
SFDR (dBc)	-85.6	-87.7	-77.2	-86.1
ENOB[10] (bits)	11.9	11.6	11.5	11.4

Table 5. Noise Spectral Density

Module	nV/rt (Hz)	dBm/Hz	dBFS/Hz
AC-coupled	9.5	-147.4	-157.5
DC-coupled	11.8	-145.6	-155.4

Note Noise spectral density is verified using a 50 Ω terminator connected to the input.

7 Normalized to 10 MHz.
8 Upper -3 dB bandwidth limited by ADC decimation filter.
9 Measured with a -1 dBFS signal and corrected to full-scale. 1 kHz resolution bandwidth.
10 Calculated from SINAD and corrected to full scale.

Figure 1. AC-Coupled Single Tone Spectrum (10.1 MHz, -1 dBFS, 1 kHz RBW), Measured

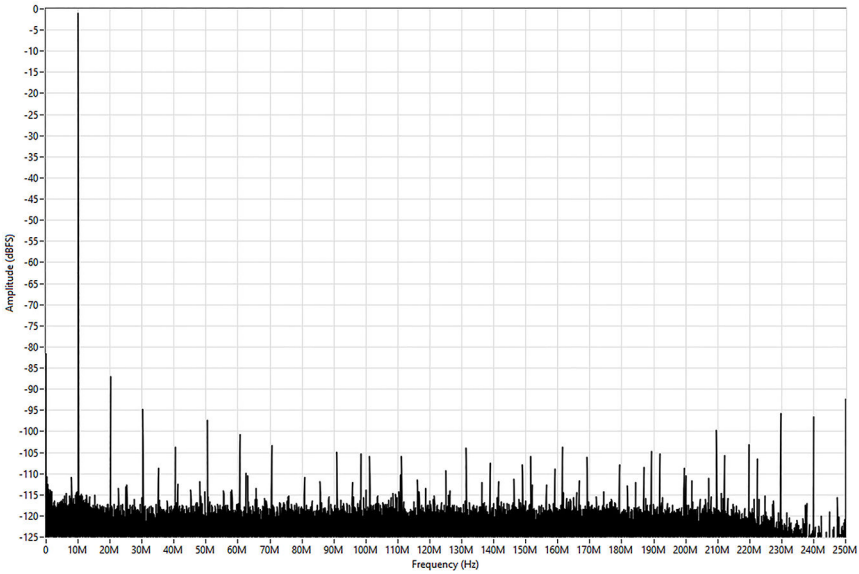


Figure 2. AC-Coupled Single Tone Spectrum (123.1 MHz, -1 dBFS, 1 kHz RBW), Measured

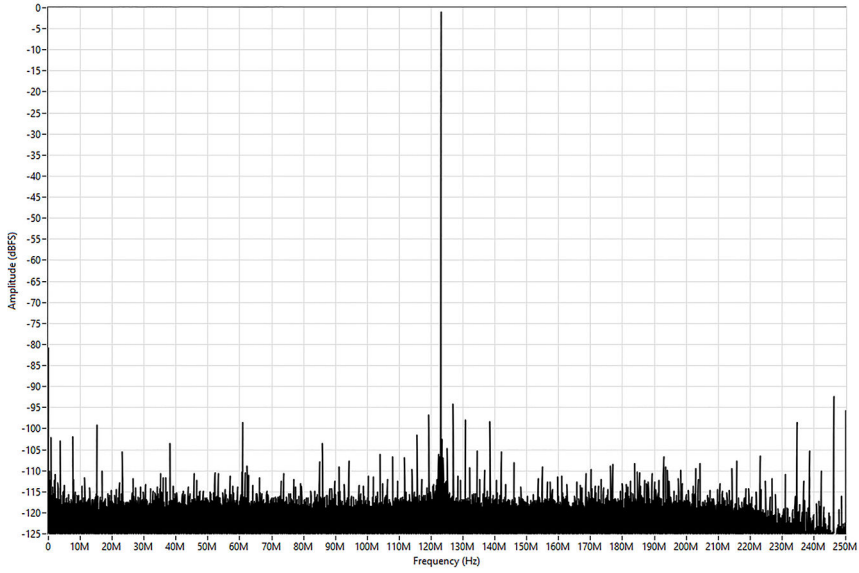


Figure 3. DC-Coupled Single Tone Spectrum (10.1 MHz, -1 dBFS, 1 kHz RBW), Measured

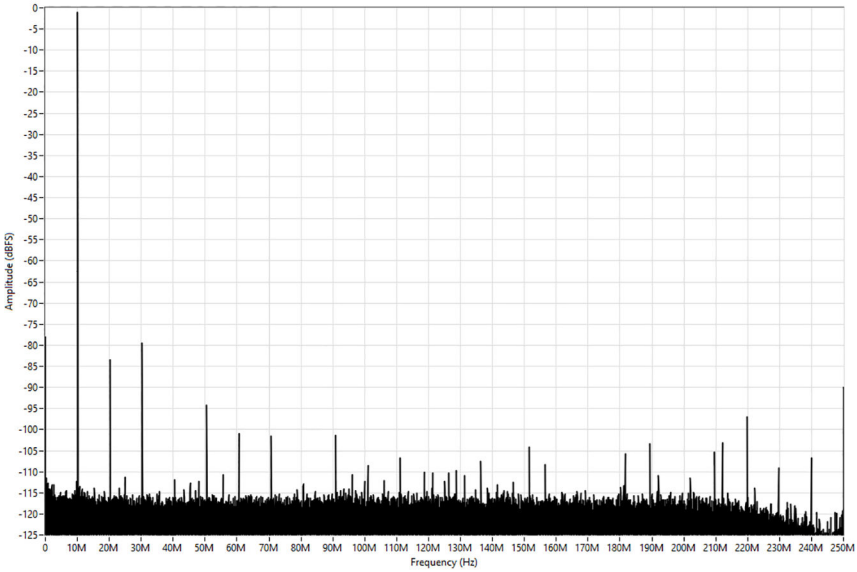
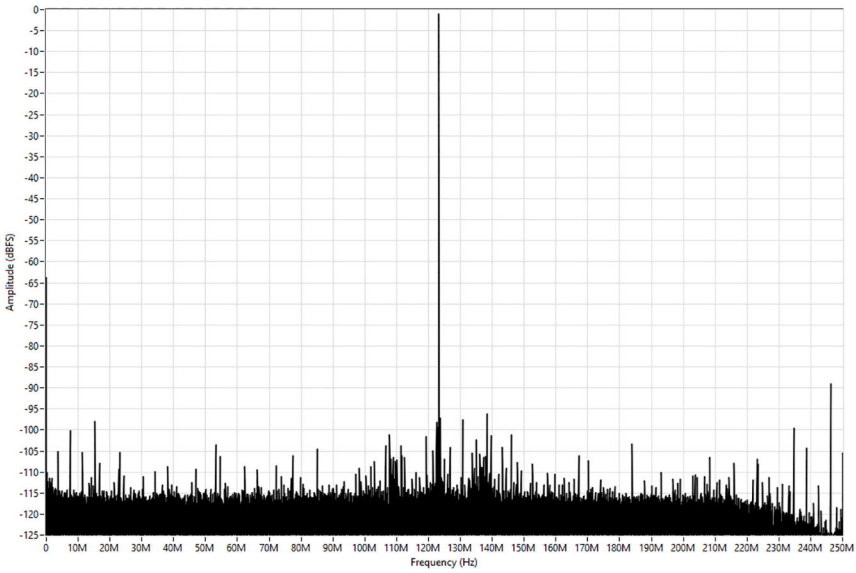


Figure 4. DC-Coupled Single Tone Spectrum (123.1 MHz, -1 dBFS, 1 kHz RBW), Measured



Channel-to-channel crosstalk AC-coupled, characteristic	
10 MHz	-87 dB
100 MHz	-89 dB
225 MHz	-85 dB
Channel-to-channel crosstalk DC-coupled, characteristic	
1 MHz	-94 dB
100 MHz	-83 dB
225 MHz	-78 dB

Figure 5. AC-Coupled Frequency Response, Measured

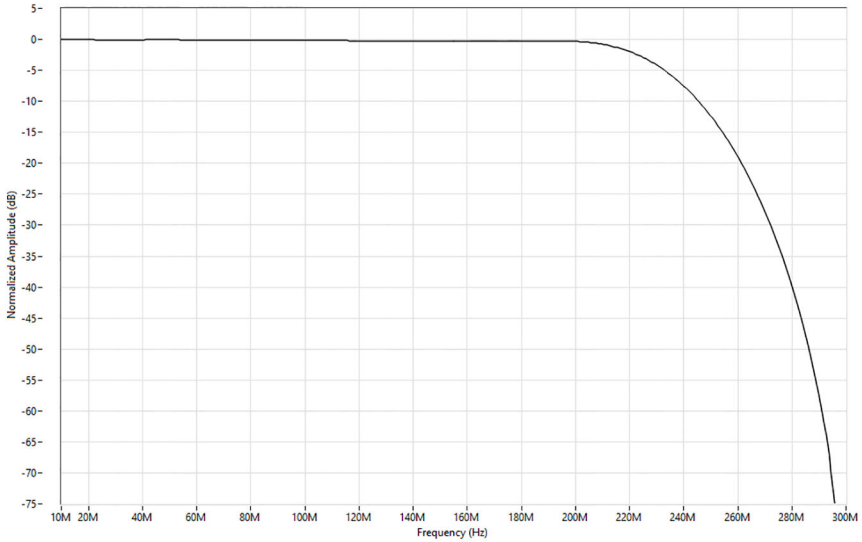


Figure 6. AC-Coupled Frequency Response Zoomed In, Measured

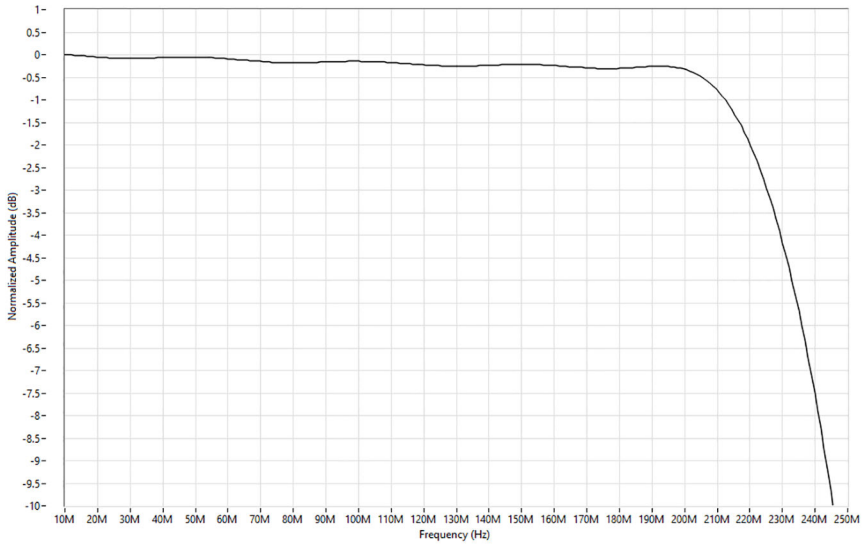


Figure 7. DC-Coupled Frequency Response, Measured

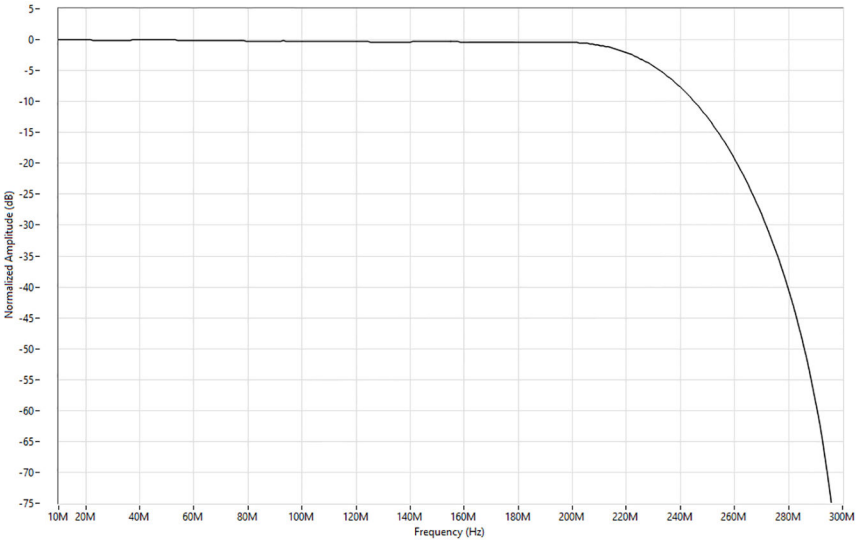


Figure 8. DC-Coupled Frequency Response Zoomed In, Measured

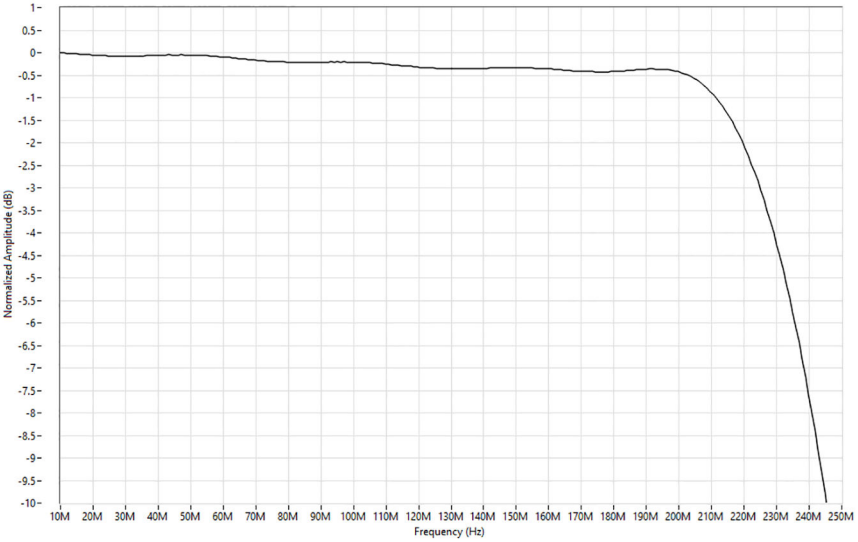
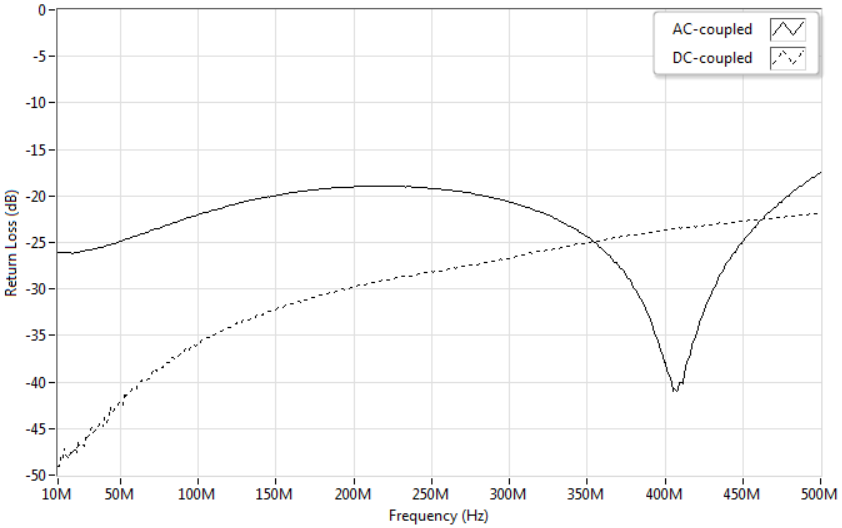


Figure 9. Input Return Loss, Measured



CLK/REF IN

General Characteristics

Connector type	SMA
Input impedance	50 Ω
Input coupling	AC
Reference input voltage range	0.3 V_{pp} to 4 V_{pp}
Sample Clock input voltage range	0.3 V_{pp} to 4 V_{pp}
Absolute maximum voltage	±12 V DC, 4 V_{pp} AC
Duty cycle	45% to 55%
Onboard reference timebase stability	±0.5 ppm
Sample Clock jitter[11]	
AC-coupled	135 fs RMS
DC-coupled	142 fs RMS

[11] Integrated from 1 kHz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

Table 6. Clock Configuration Options

Clock Configuration	External Clock Type	External Clock Frequency	Description
Internal Reference Clock[12]	—	—	The internal Sample Clock locks to an onboard voltage-controlled temperature compensated crystal oscillator (VCTCXO).
Internal PXI_CLK10	—	10 MHz	The internal Sample Clock locks to the PXI 10 MHz Reference Clock, which is provided through the backplane.
External Reference Clock (CLK/REF IN)	Reference Clock	10 MHz[13]	The internal Sample Clock locks to an external Reference Clock, which is provided through the CLK/REF IN front panel connector.
External Sample Clock (CLK/REF IN)	Sample Clock	1 GHz [14]	An external Sample Clock can be provided through the CLK/REF IN front panel connector.

[12] Default clock configuration.
[13] The PLL Reference Clock must be accurate to ±25 ppm.
[14] The ADC sample rate is 500 MS/s with a 1 GHz clock.

Figure 10. AC-Coupled Phase Noise with 182.6 MHz Input Tone, Measured

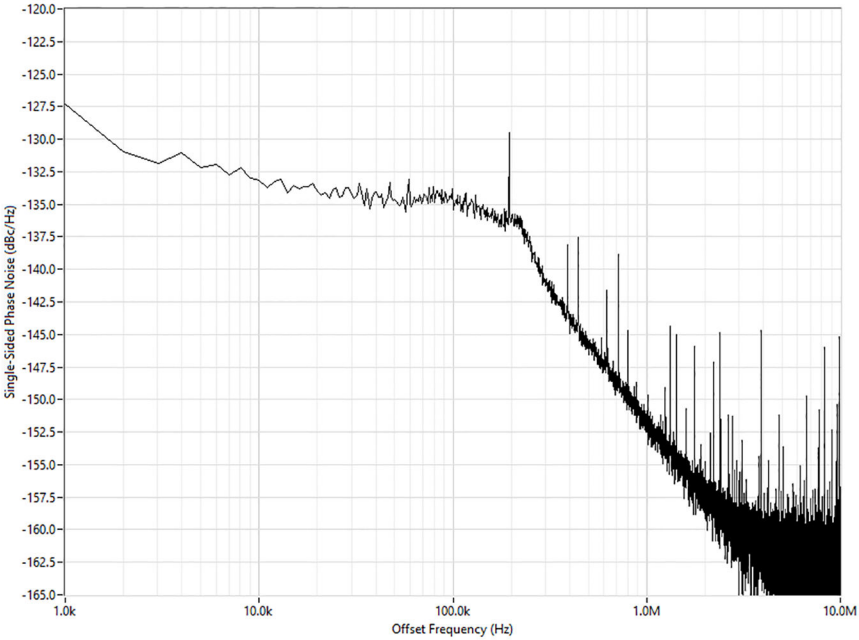
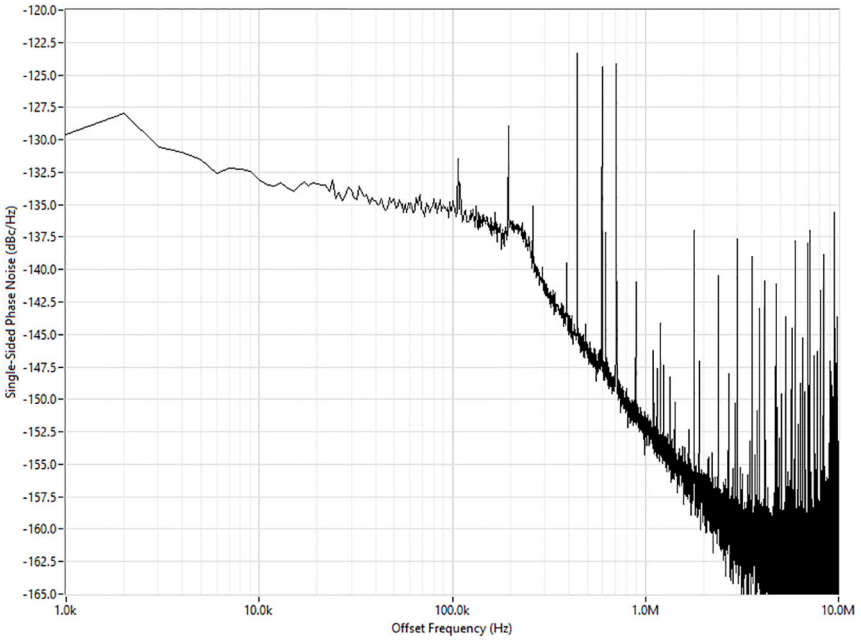


Figure 11. DC-Coupled Phase Noise with 182.6 MHz Input Tone, Measured



Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	500 g (17.6 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[15]
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 4 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

[15] The PXIe-5763 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the *PXI Chassis Manual* for specifications to determine the ambient temperature ranges your chassis can achieve.

Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

TCLK Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample Clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help* within the *FlexRIO Help*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample Clocks of each module.
- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample Clock.

Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[16]	
AC-coupled	130 ps, measured
DC-coupled	140 ps, measured
Skew after manual adjustment	≤10 ps, measured
Sample Clock delay/adjustment	1.5 ps

[16] Caused by clock and analog delay differences. No manual adjustment performed. Tested with a PXIe-1085 chassis with a 24 GB backplane with a maximum slot to slot skew of 100 ps. Measured at 23 °C.

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